A Novel Technique for Contamination Analysis around the Bevel and Edge Exclusion Area of 200 and 300mm Silicon Wafers

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February 27, 2003
SPIE **Process and Materials Characterization and Diagnostics in IC Manufacturing II**

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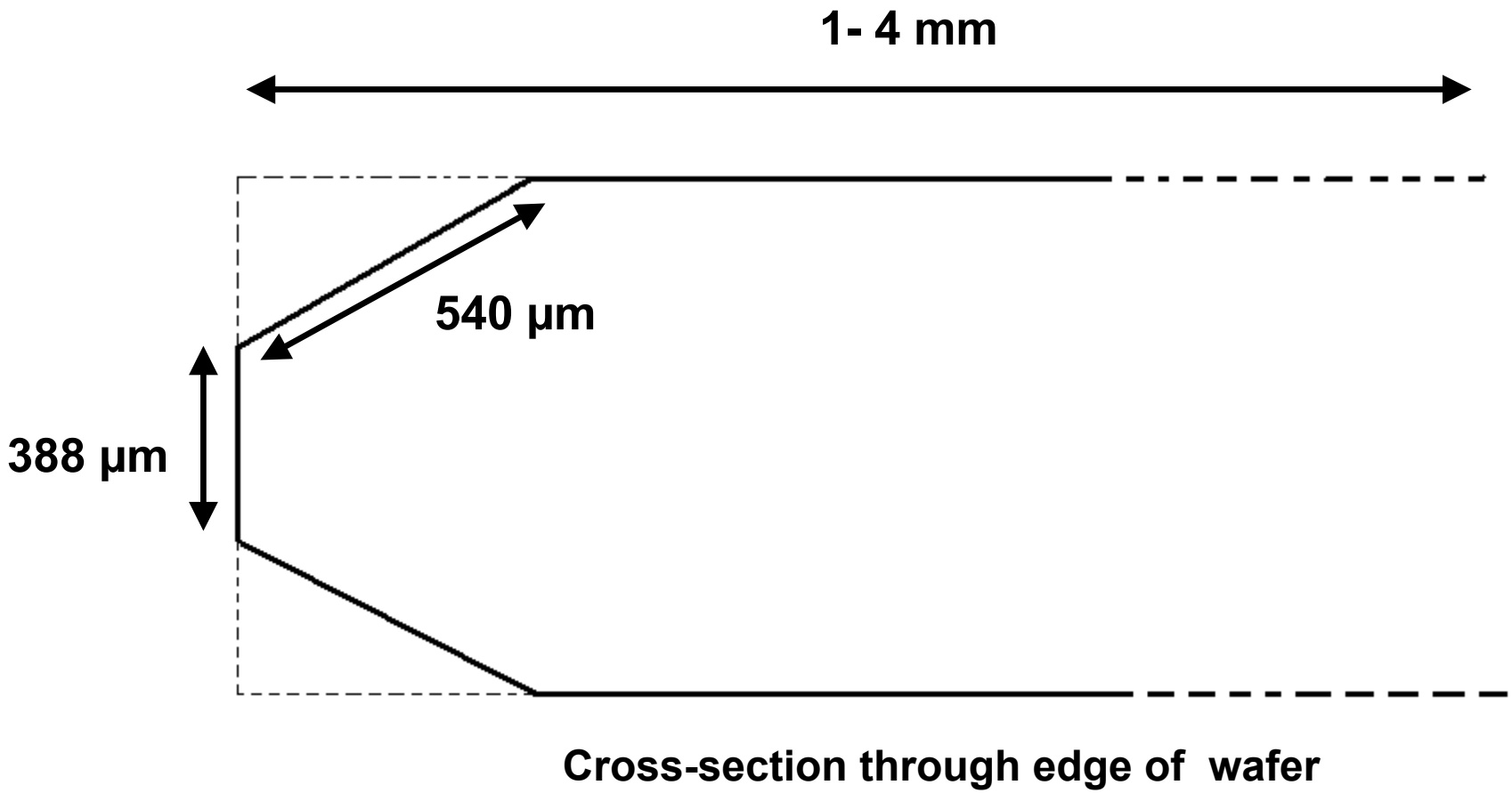
What is the Edge Exclusion and Bevel Area of a Wafer?



Cross-section through edge of wafer

Approximate values based on T/4 wafer edge profile
SEMI M1-0701
Figure not to scale

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Why Do We Need to Know About Contamination in the Bevel/Edge Exclusion Area of a Wafer?

- **Monitor the efficiency of a film stripping tool (for example, wafer backside cleaning)**
- **Monitor for contamination**
  - Test for contamination transfer from wafer alignment/centering pins
  - Contamination from direct contact between the wafer edge and cassette
  - Concern with contamination diffusing from edge to active sites on the wafer

Can Typical Analytical Techniques Measure the Bevel Area?

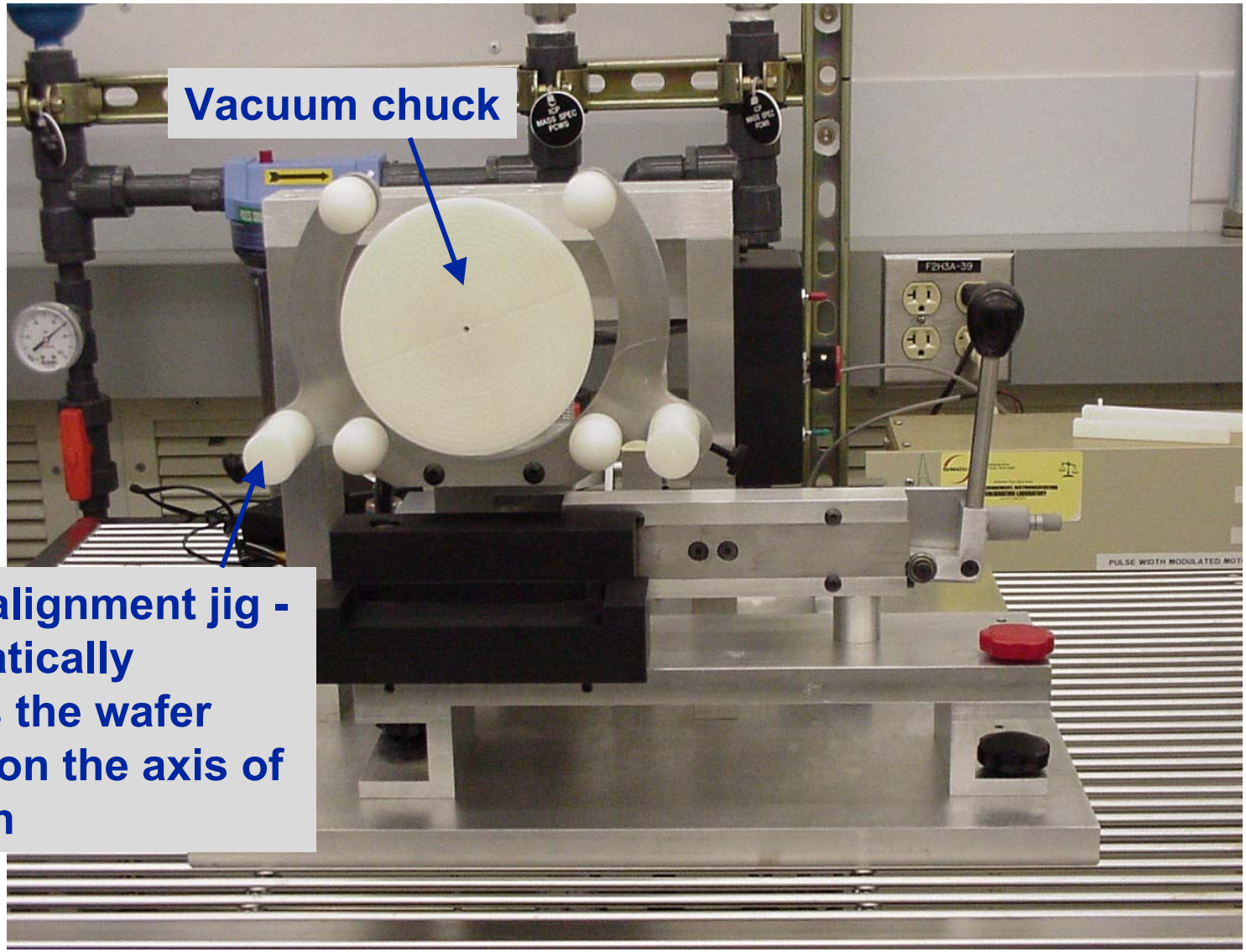
- TXRF can not operate that close to the edge due to scatter of incident radiation
- TOF-SIMS not easily used on the angled bevel
- VPD-ICP-MS would expose the entire wafer to HF vapor
- DADD (direct acid drop decomposition) ICP-MS lacks control over analysis of the bevel

Explain ICP, VPD, TXRF?

Our Solution…

- Support a wafer vertically
- Bring an extraction solution up to the desired depth on the edge of the wafer
- Rotate the wafer's edge slowly through the extraction solution (~ 8 minutes/rotation)
- Analyze the solution for trace metals by ICP-MS

Front View



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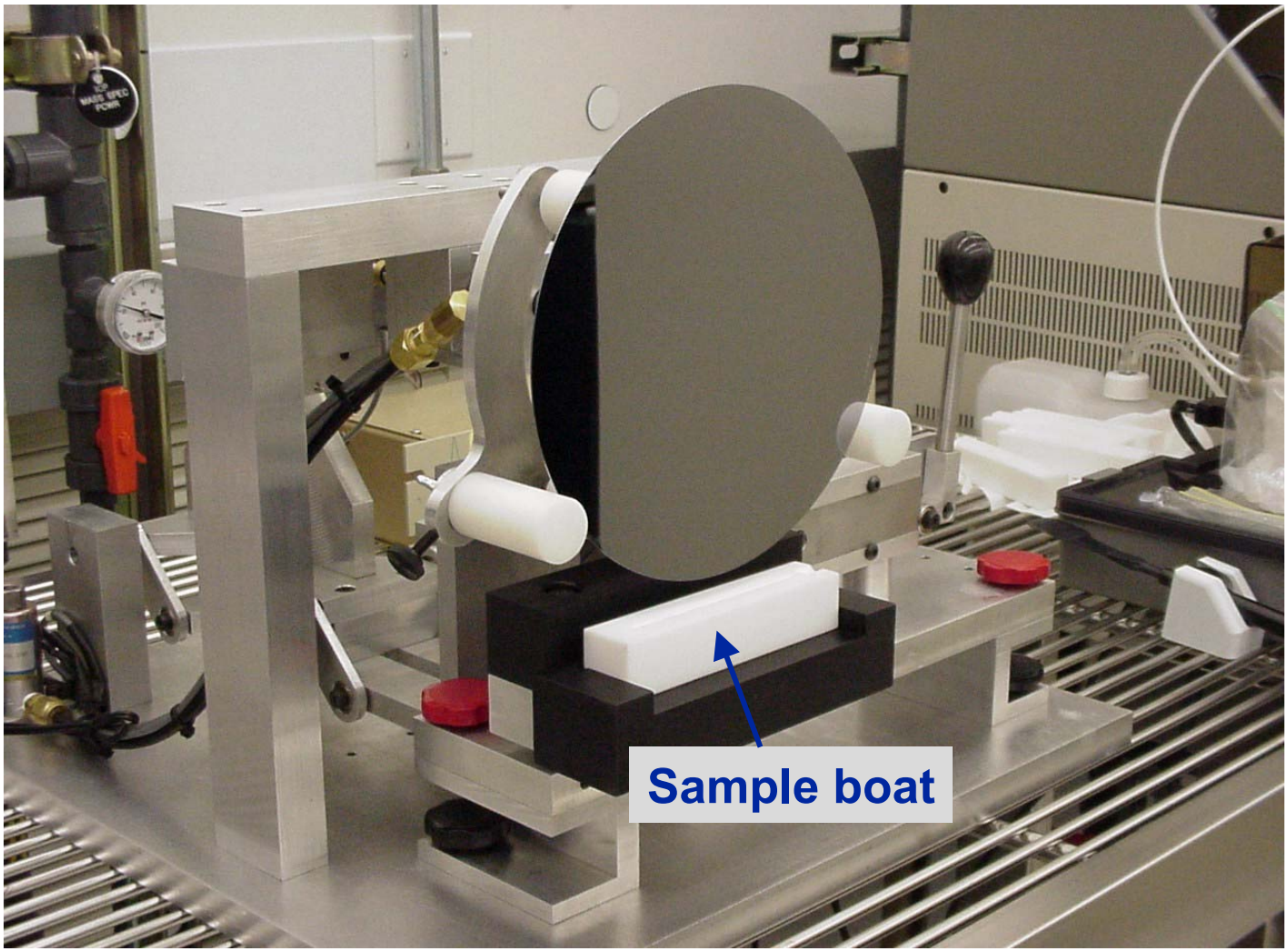
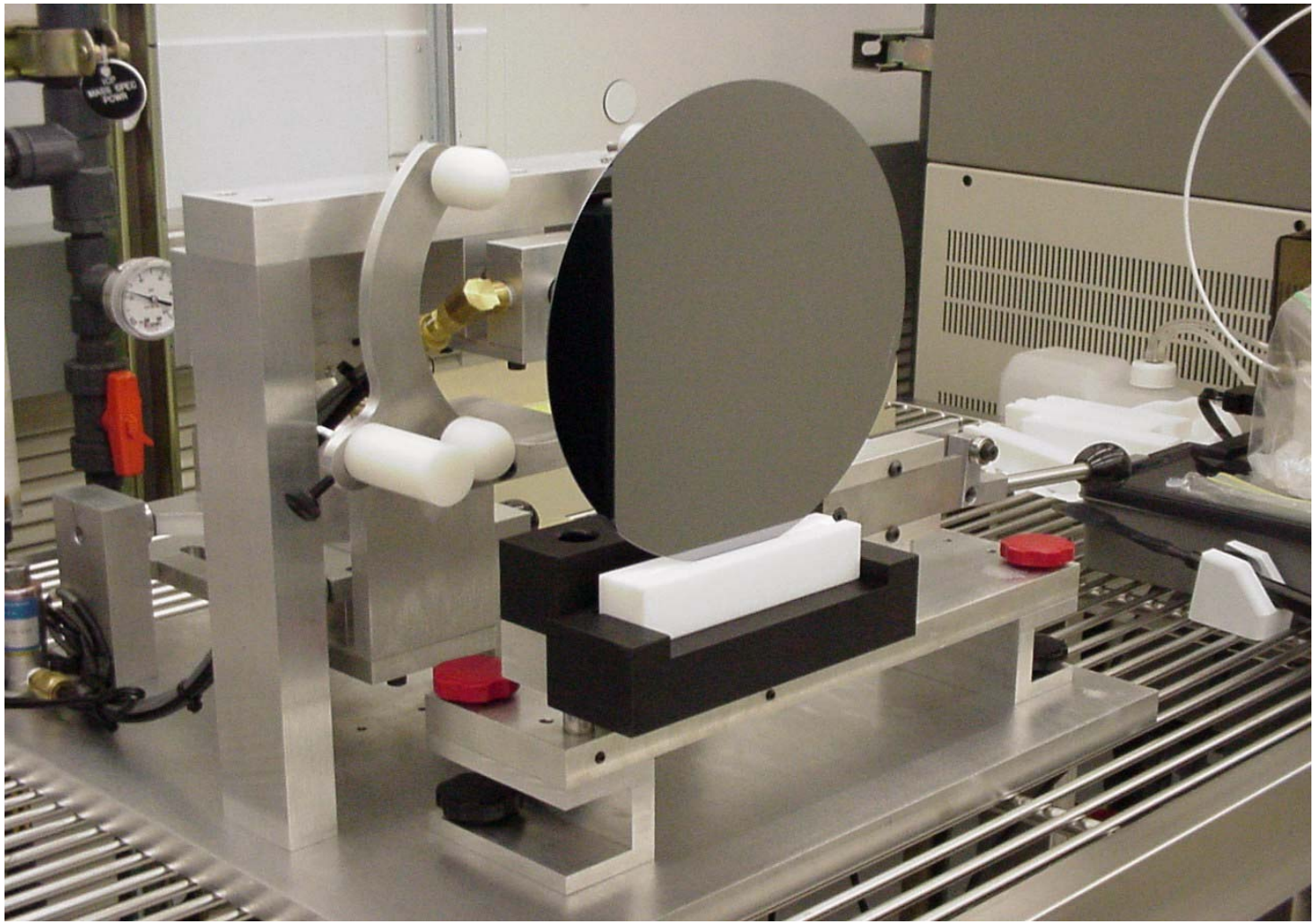
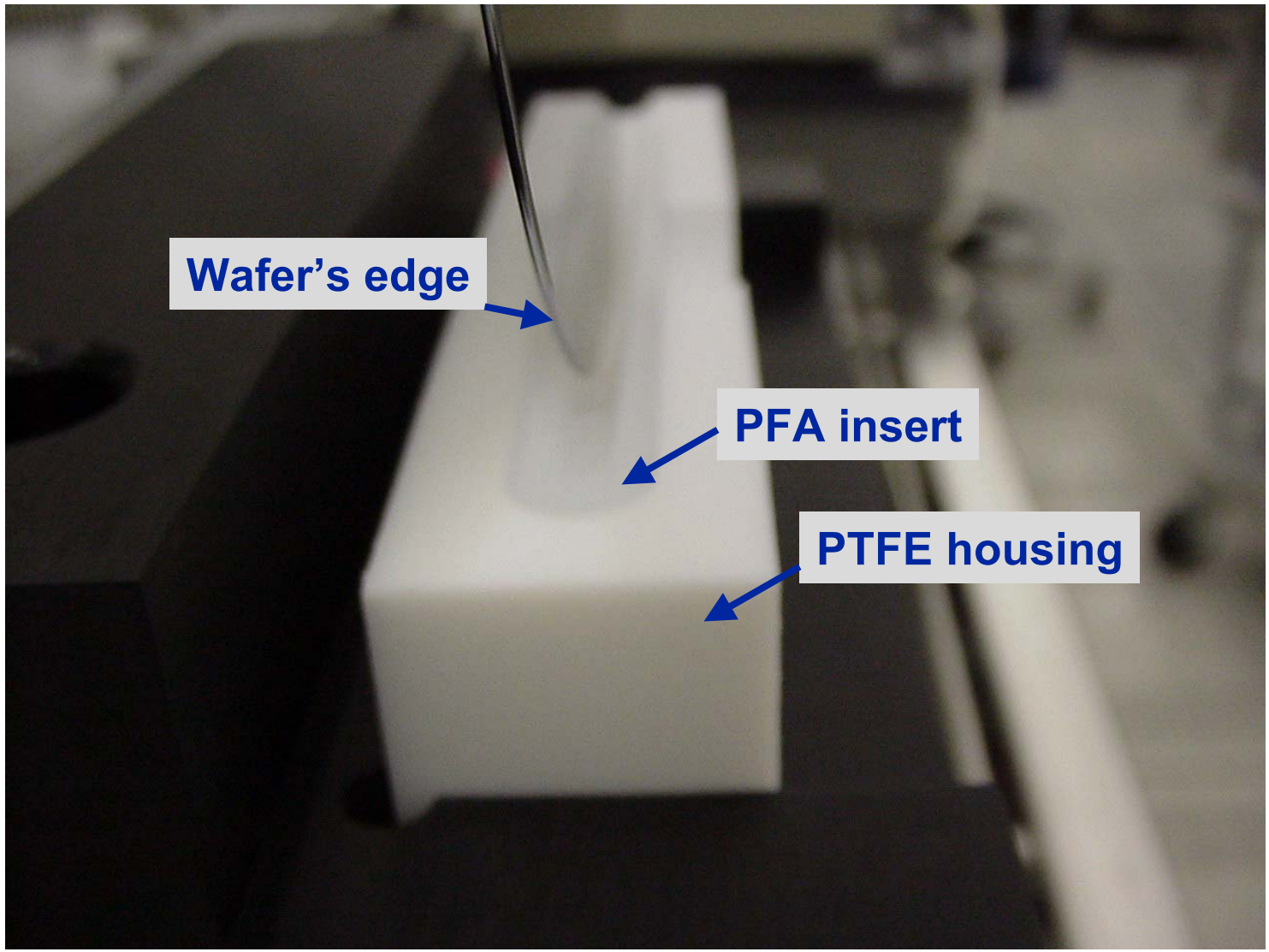
Wafer in Alignment Jig – centers the wafer for vacuum suspension



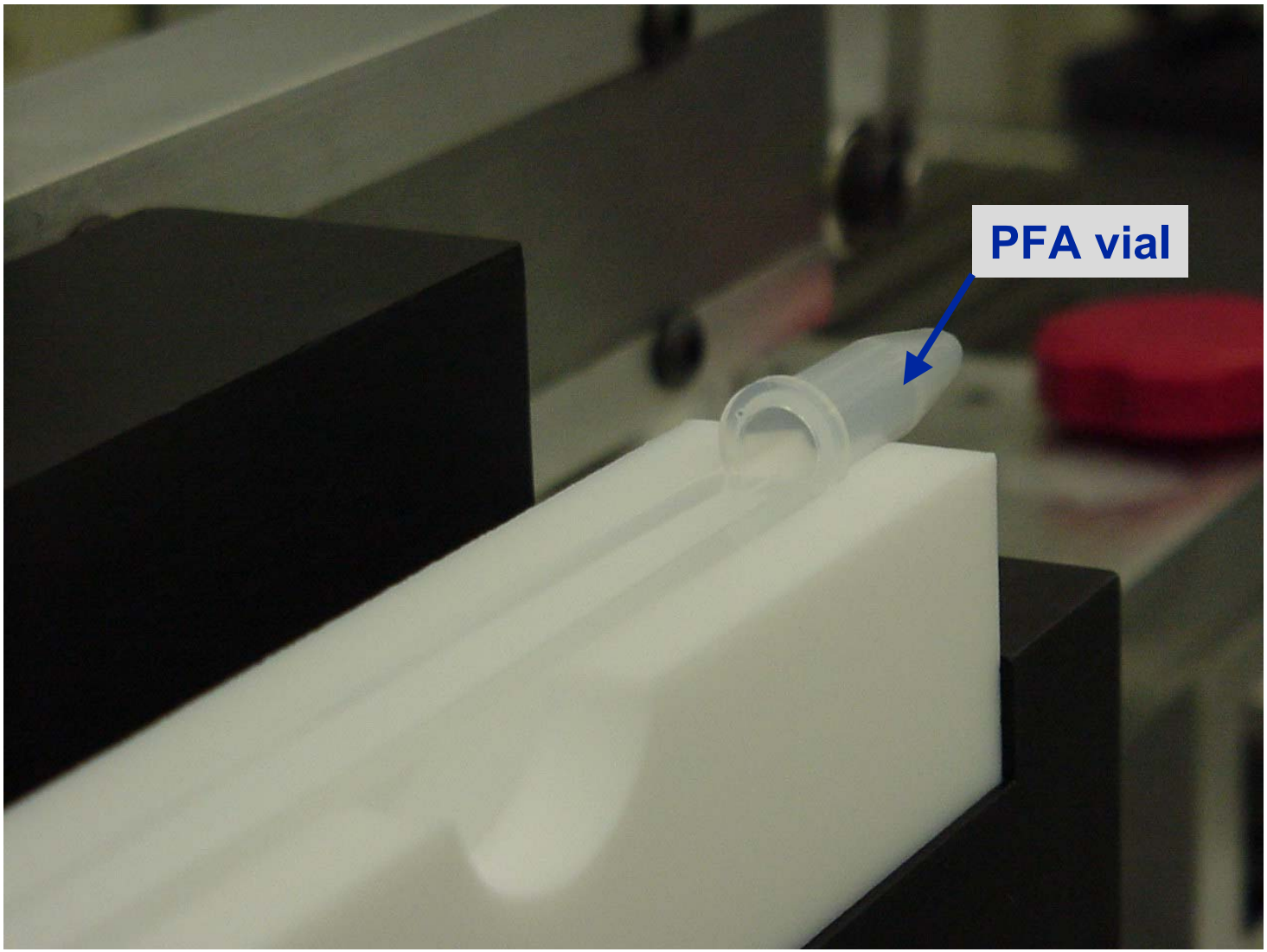
Sample Boat Raised and Alignment Jig Withdrawn



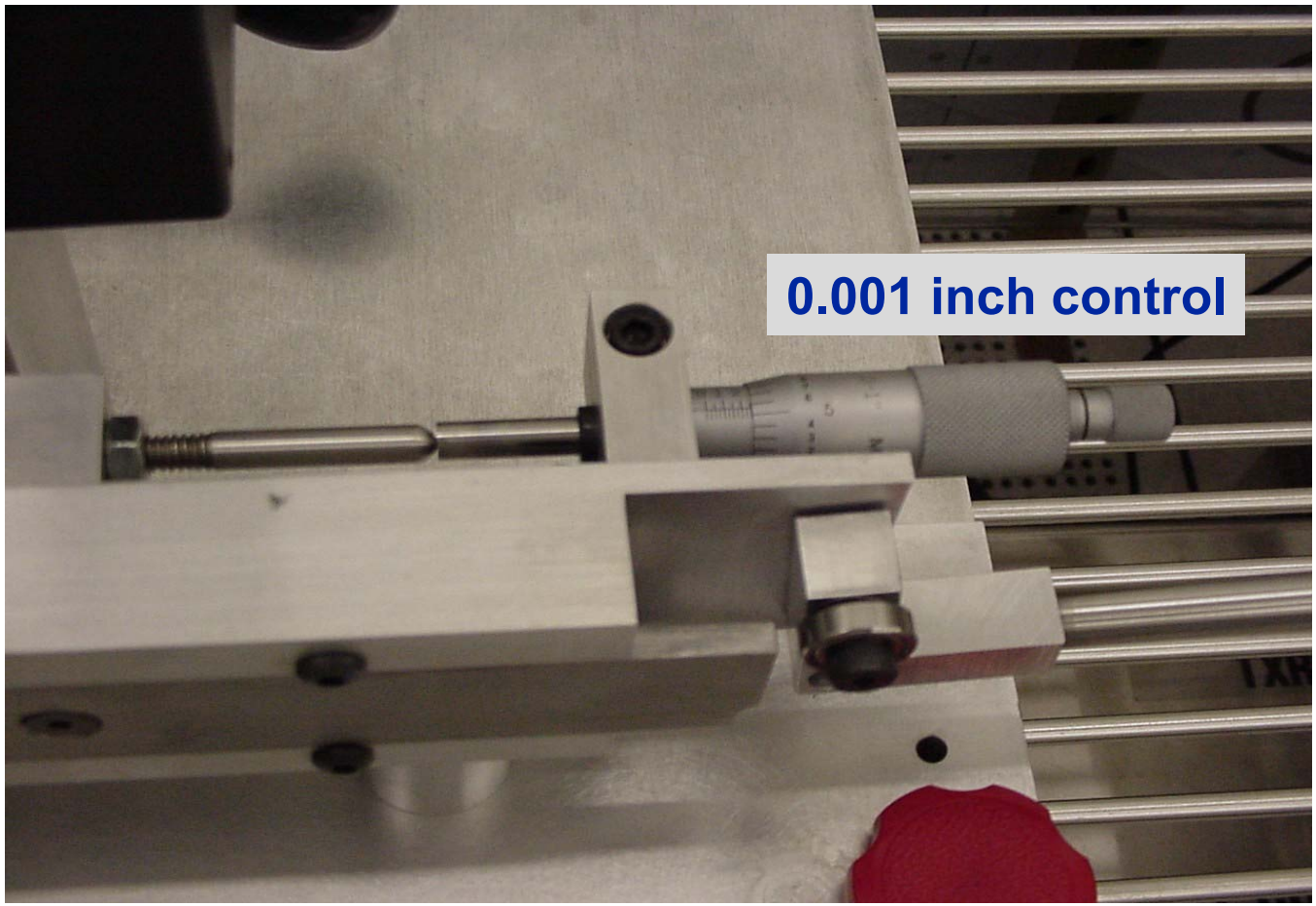
Edge View of Wafer in Sample Boat



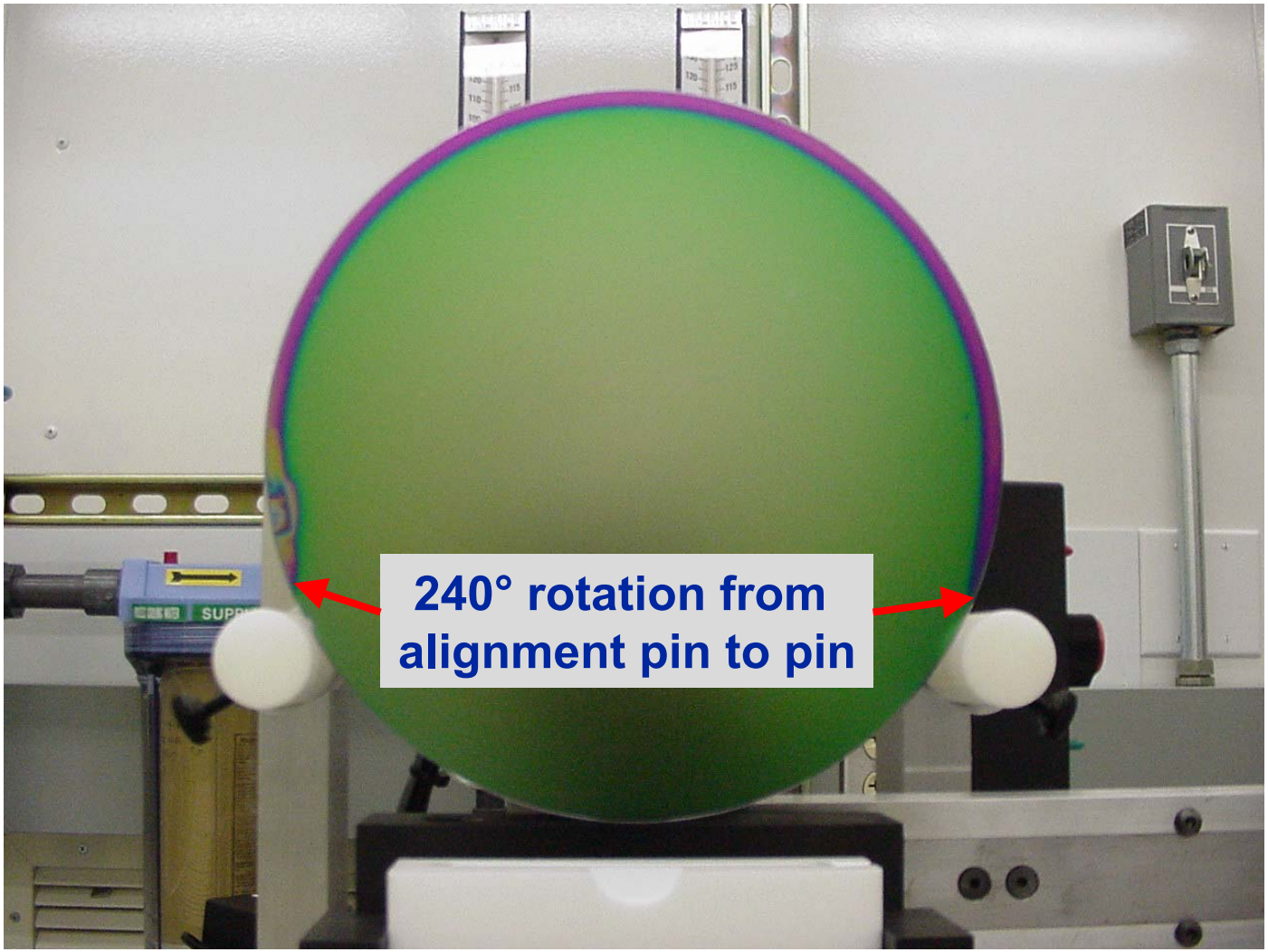
500 µL Sample Vial on Chemical Boat



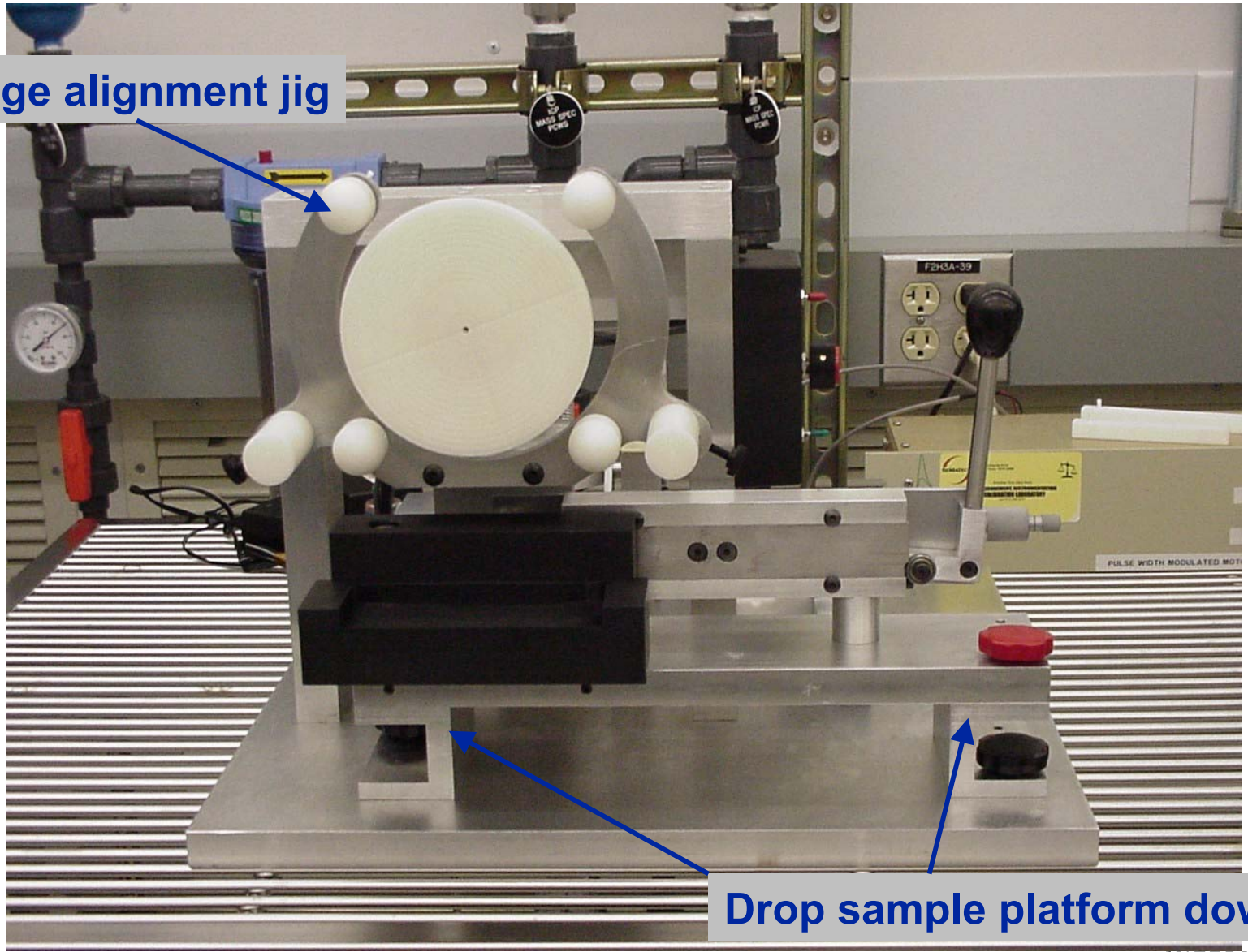
Micrometer Fine Adjustment of the Sample Boat - provides variable depth measurement of the edge exclusion region



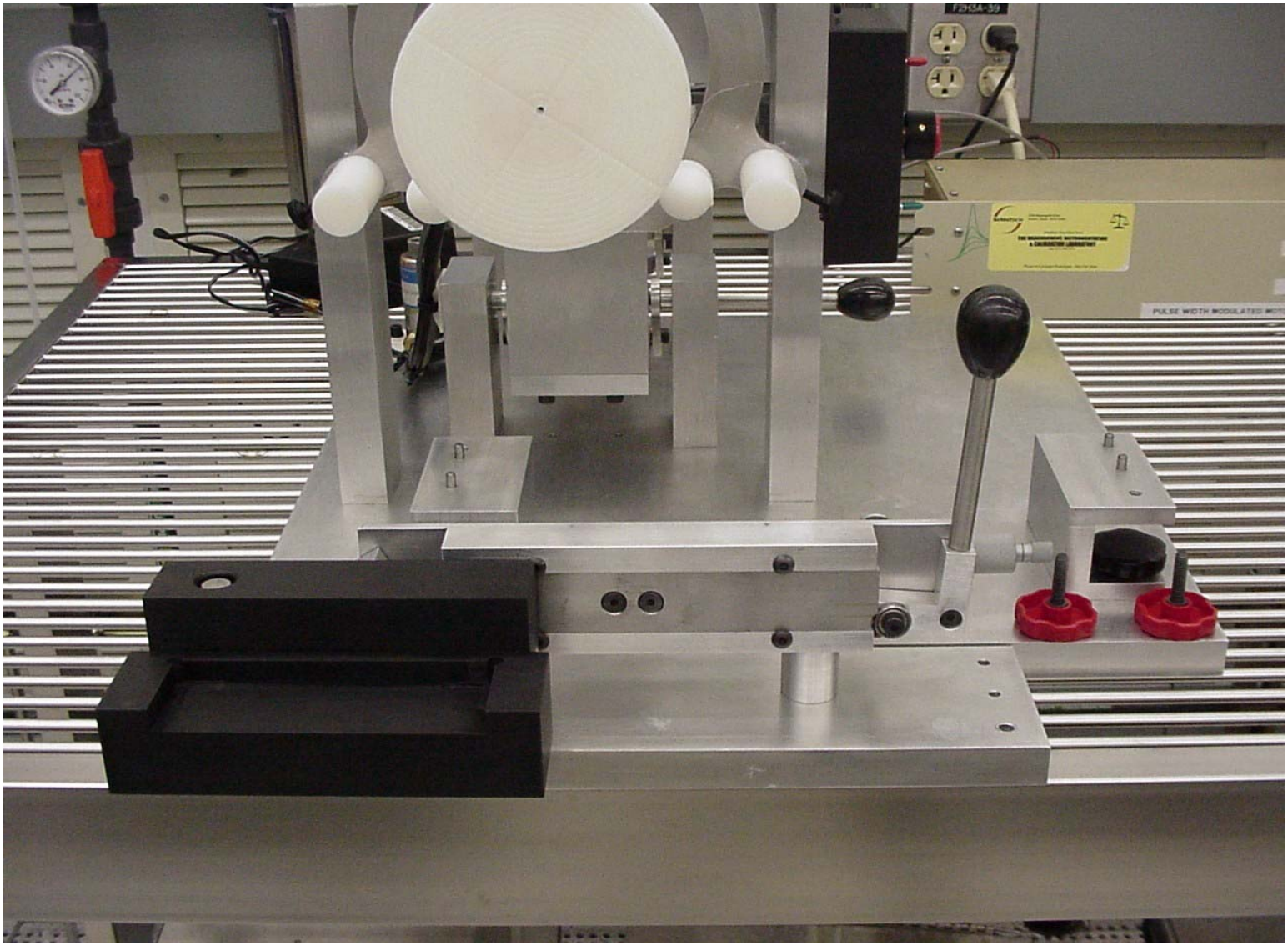
Example of 5mm Edge Analyzed with a 5500 Å Silicon Dioxide Wafer



Conversion from 200mm to 300mm



Top Half of Sample Platform Removed



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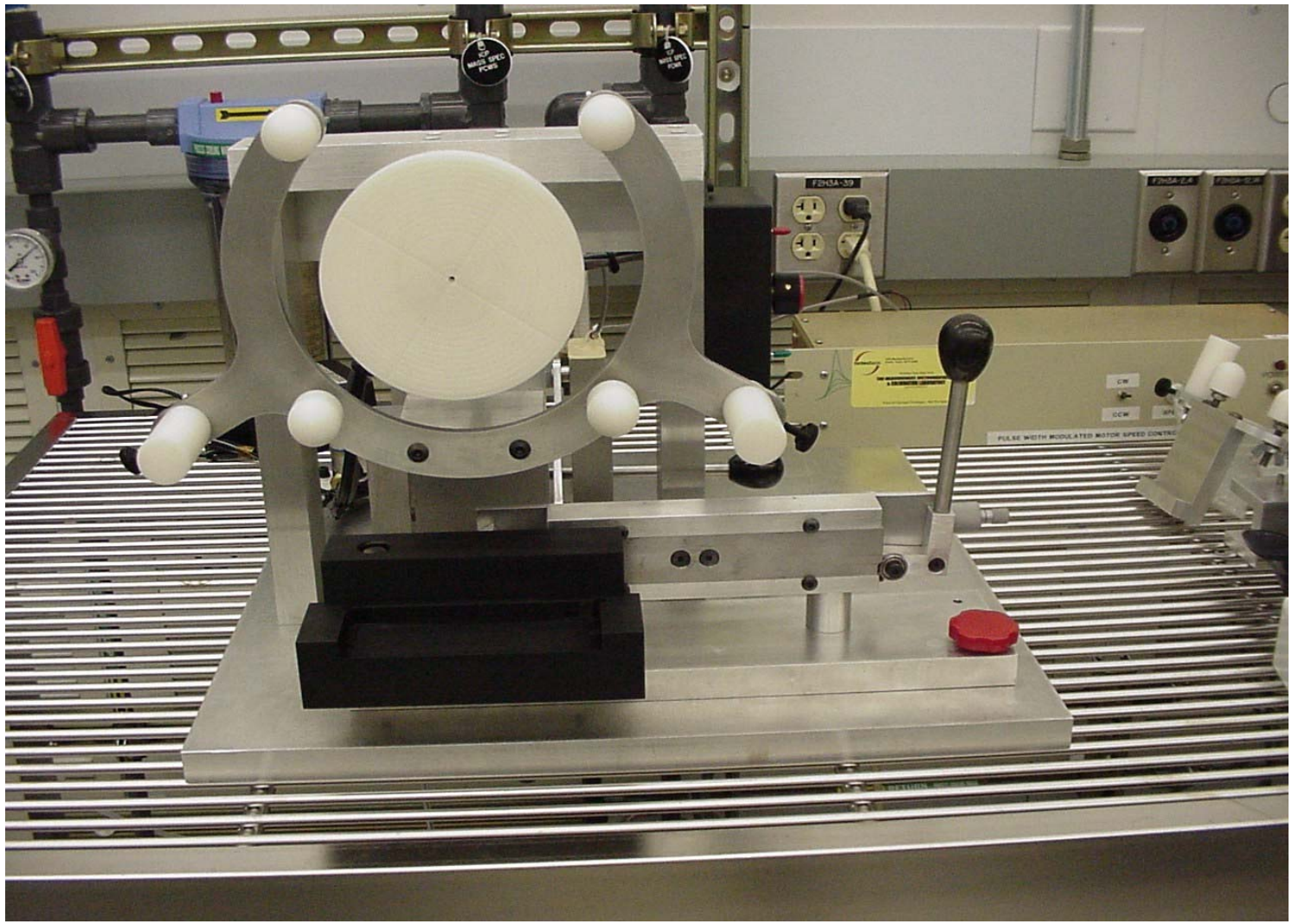
300mm Wafer Setup

5 minute change-over process



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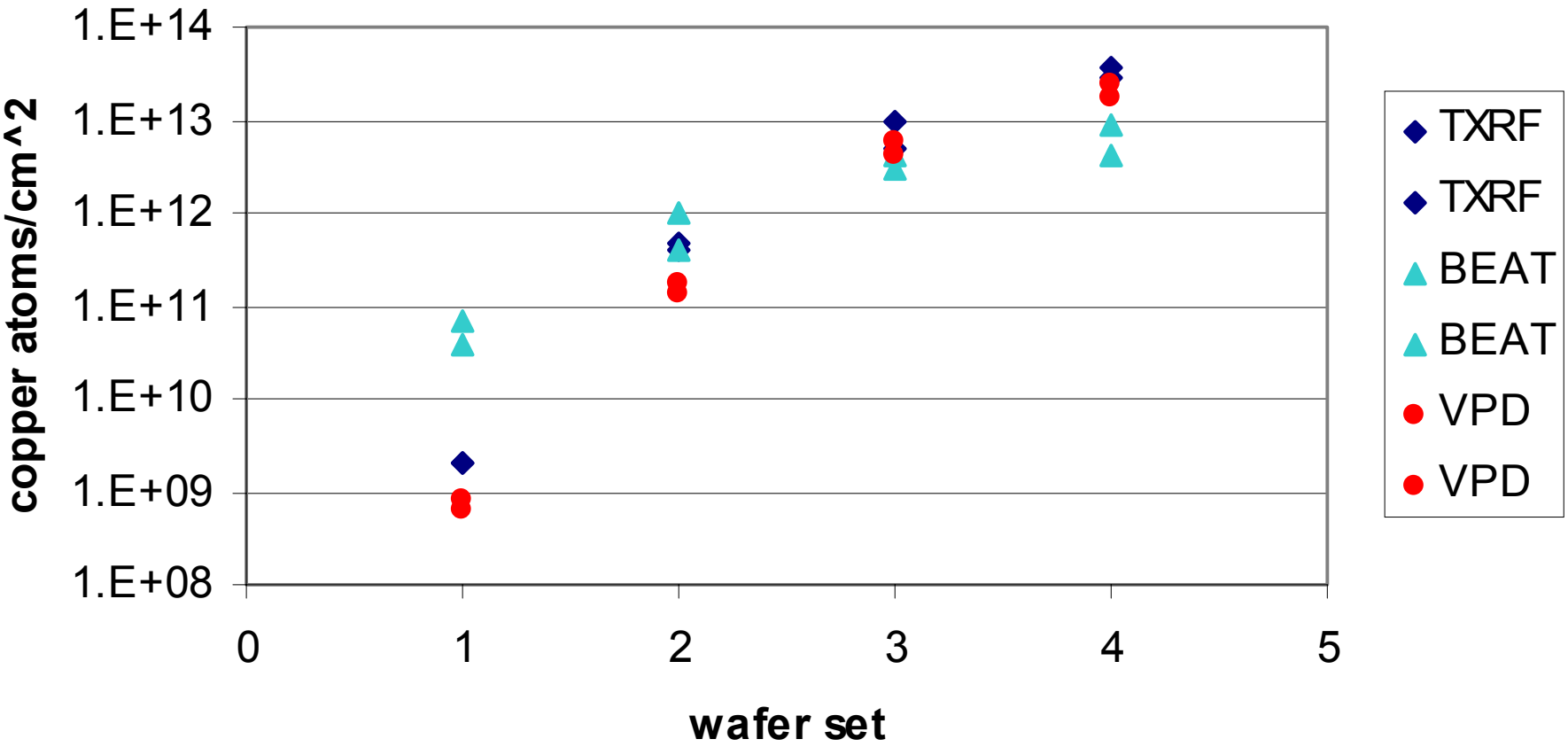
Why is the Semiconductor Industry Concerned with Copper?

- **Copper replacing aluminum for on-chip wiring between devices**
  - Improves reliability of devices (longer lasting, less problems with electromigration)
  - Lower resistance
    - Improves device speed (T=RC)
    - Reduces power loss ($P=i^2R$)
- **Problem: Copper has a high mobility in silicon**
  - Without proper isolation it can move from anywhere to an active device (i.e., a transistor)
  - Reduces lifetime/diffusion length of carriers (a carrier trap)-making a non-functional device

Experiment

- Contaminate wafers with copper
- Nine point TXRF (Technos 630T) analysis
- Do bevel/edge analysis with a 4mm included edge (repeat to look for extraction efficiency)
- Analyze remainder of wafers by VPD-ICP-MS (Mesa-Tek and Agilent 4500)
- Remeasure by TXRF to look for VPD extraction efficiency

Results from Techniques Comparison



Recovery Test of Wafer's Edge

Wafer	edge pass 1	edge pass 2	% recovery
1	3.7 E10	7.6 E09	79.8
2	6.8 E10	5.0 E09	92.6
3	4.1 E11	1.8 E10	95.5
4	1.0 E12	1.7 E10	98.4
5	3.1 E12	4.5 E10	98.5
6	4.0 E12	3.9 E11	90.3
7	4.0 E12	1.6 E11	96.0
8	8.6 E12	1.2 E12	85.5

Copper concentration in atoms/cm^2 based on a 4mm edge analyzed

Recovery Test of VPD Technique

spiked wafer	TXRF pre VPD	VPD-ICP-MS results	TXRF post VPD	% VPD recovery
1	4.1 E11	1.7 E11	1.1 E11	72.8
2	4.8 E11	1.3 E11	1.0 E11	78.7
3	4.8 E12	6.0 E12	1.5 E11	96.9
4	9.3 E12	4.2 E12	2.5 E11	97.3
5	3.8 E13	2.3 E13	1.8 E12	95.3
6	2.8 E13	1.7 E13	4.2 E11	98.5

Copper concentration in atoms/cm^2

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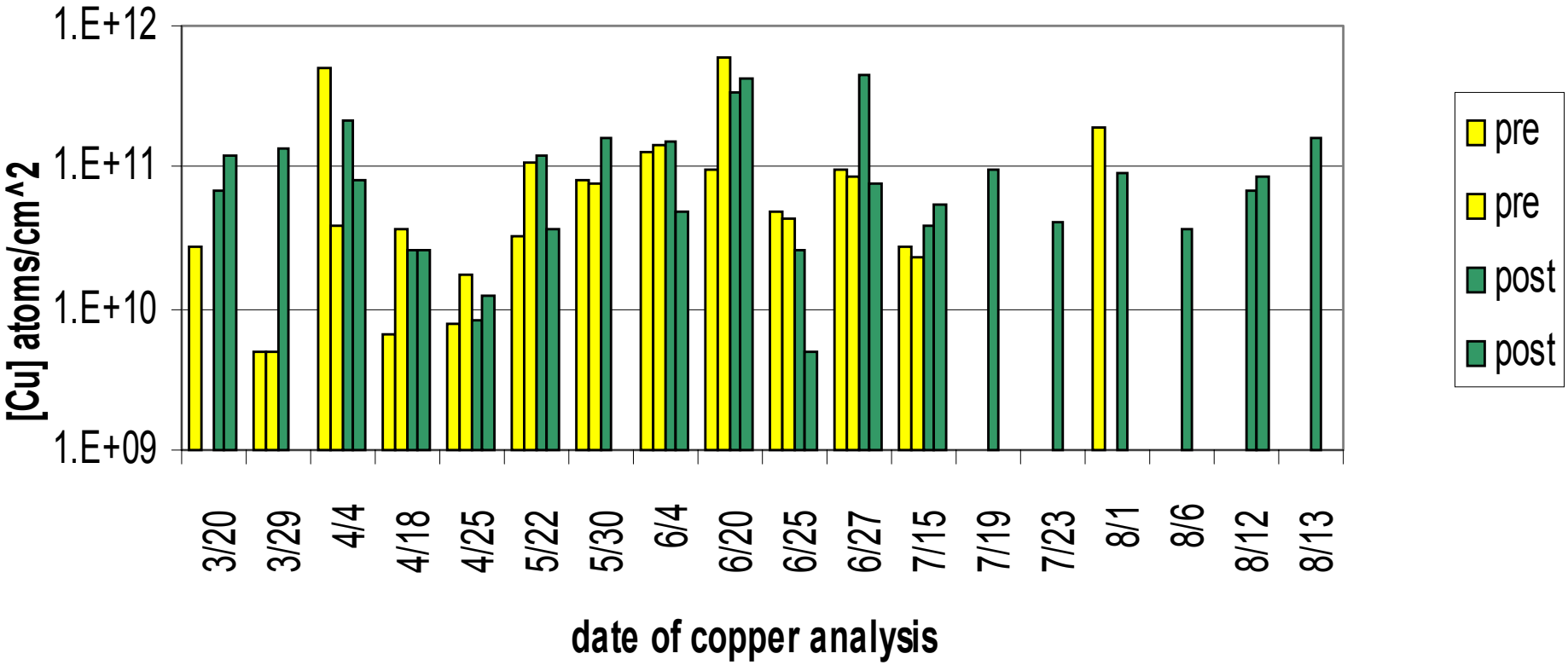
Pre and Post Copper Analysis of a Lithography Process Tool



Hafnium Contamination from Edge Contact in a Furnace

	Contact with furnace sled	Control wafer
Na	4.1E10	< 4E10
Al	2.3E11	8.5E10
Hf	2.4E10	< 7E08

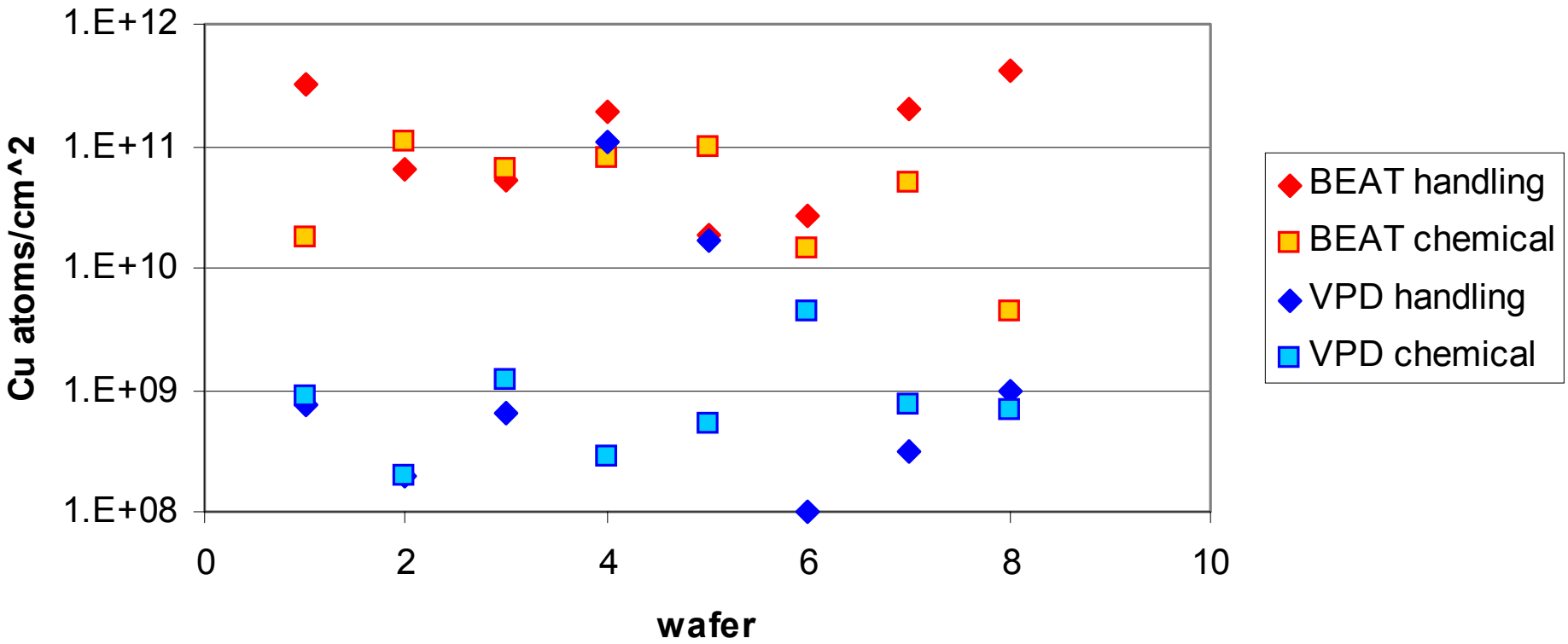
All results are in atoms / cm^2

Edge Analysis of Cassettes from High-*k* Deposition Tool

	High-*k* chamber cassette	Other chamber cassette
Na	< 4E10	< 4E10
Al	5.1E12	3.1E11
Hf	3.0E10	1.2E10

All results are in atoms / cm^2

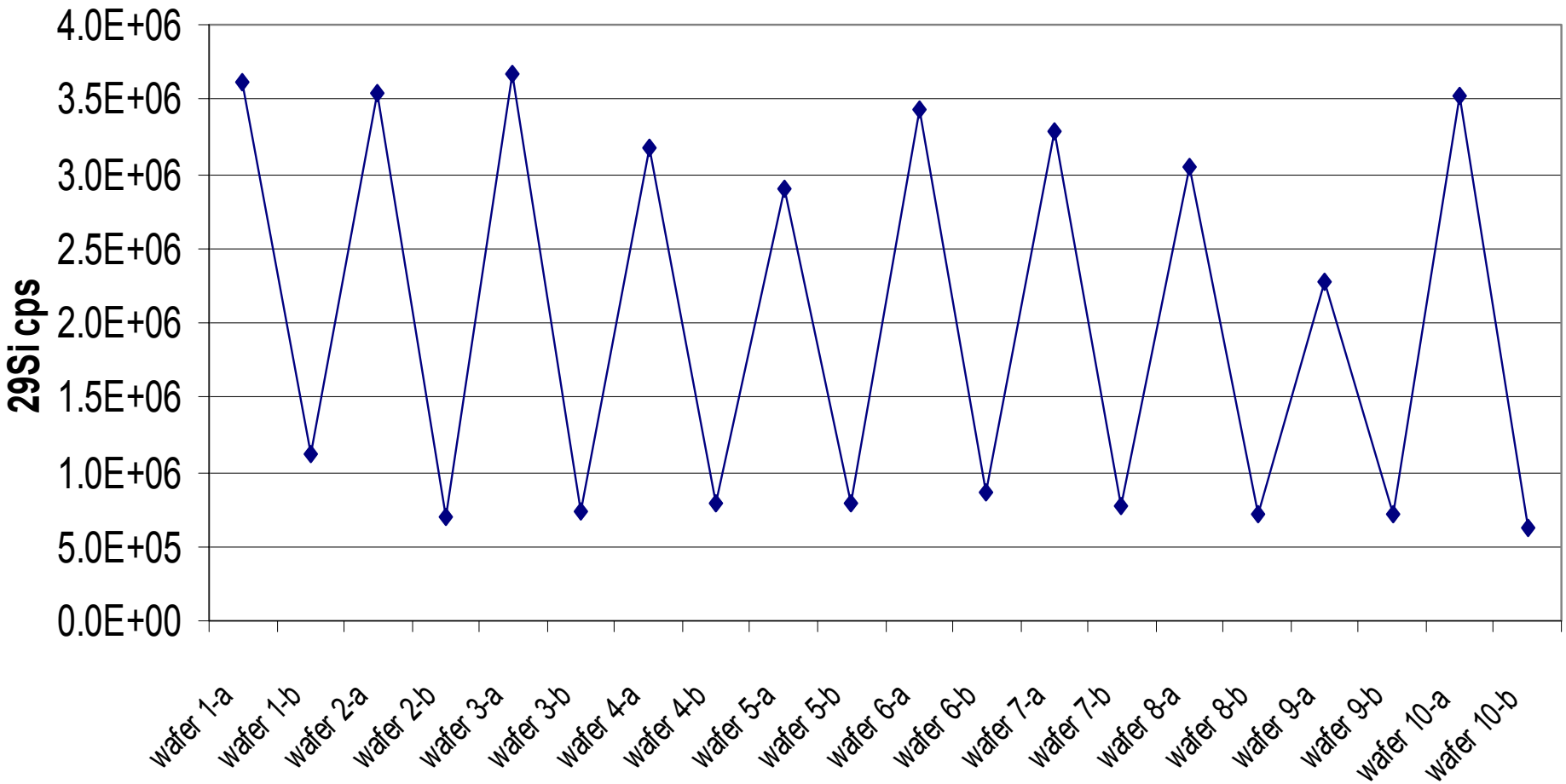
VPD and BEAT Data for the Same Wafers from 300mm Cleans Tool



Cause for higher copper background at blank

- **28Si19F16O = m/z 63 other isotopes add up to m/z 65**
- **Investigate with high-resolution ICP-MS**
- **Contamination from BEAT?**
  - test

Silicon Counts (Edge Analyzed Samples)



"a" designates the first pass of the wafer through the scan solution
"b" designates the second pass of the wafer through the scan solution

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Examples of BEAT-ICP-MS Detection Limits

	2mm edge 200mm	4mm edge 200mm	2mm edge 300mm	4mm edge 300mm
Sodium	2E10	1E10	2E10	8E09
Aluminum	4E10	2E10	3E10	1E10
Iron	9E09	5E09	6E09	3E09
Nickel	1E10	6E09	8E09	4E09
Copper	2E09	1E09	1E09	6E08
Hafnium	5E08	2E08	3E08	2E08

units are atoms/cm^2

Conclusions

- We have developed a novel method of measuring trace metal contamination around the bevel and edge of a silicon wafer
- Results from this new technique compare very well with established techniques (TXRF and VPD-ICP-MS)
- We need to determine if the signal we see from copper on the control wafers is real

Acknowledgments

- **Meredith Beebe** of ISMT assisted in collecting data
- **Gary Donahue** of Universal Engineering, custom design and machining
- **Russ Saville** of Savillex, custom Teflon work
- **Michael Pendley** of ISMT, variable speed control box